



ASE GROUP

Packaging Innovation for our Application Driven World

Rich Rice
ASE Group
March 14th, 2018

MEPTEC / IMAPS Luncheon Series



What We'll Cover

- Semiconductor Roadmap Drivers
- Package Development Thrusts
- Collaboration
- Summary



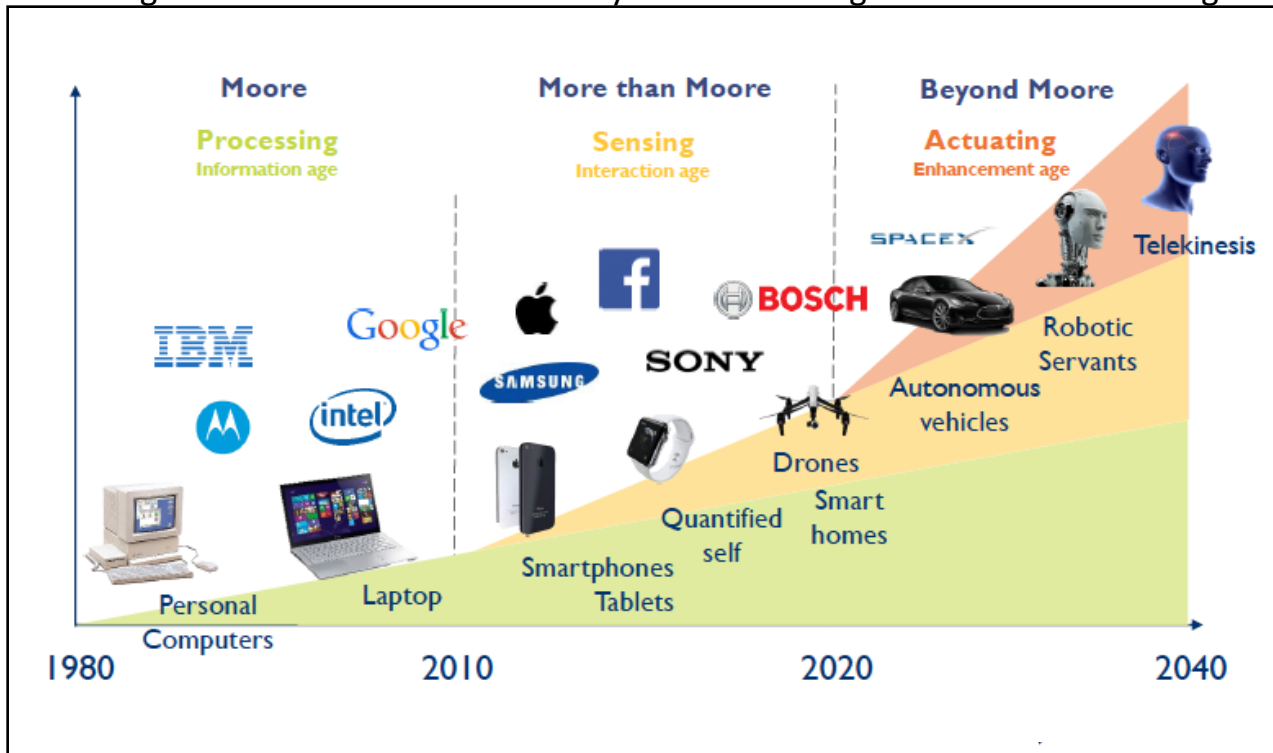
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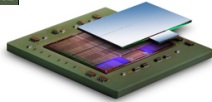
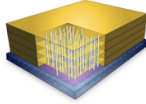
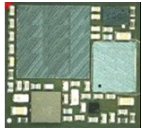
Semiconductor Roadmap Drivers

- Moving from Moore's Law driven to system level integration driven technologies.



Source: Yole 2.5D/3D Business Update 2017

IC and Systems Drivers Converge



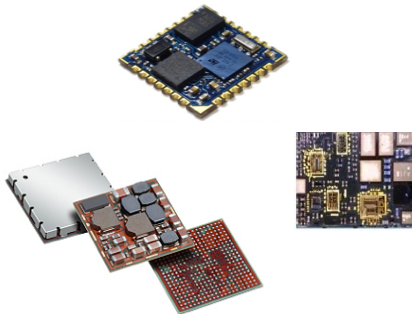
**IC Developer
Driven**

Device Package

SiP & SiM
OSAT & EMS
Integration & Miniaturization
Value Up & Cost Down

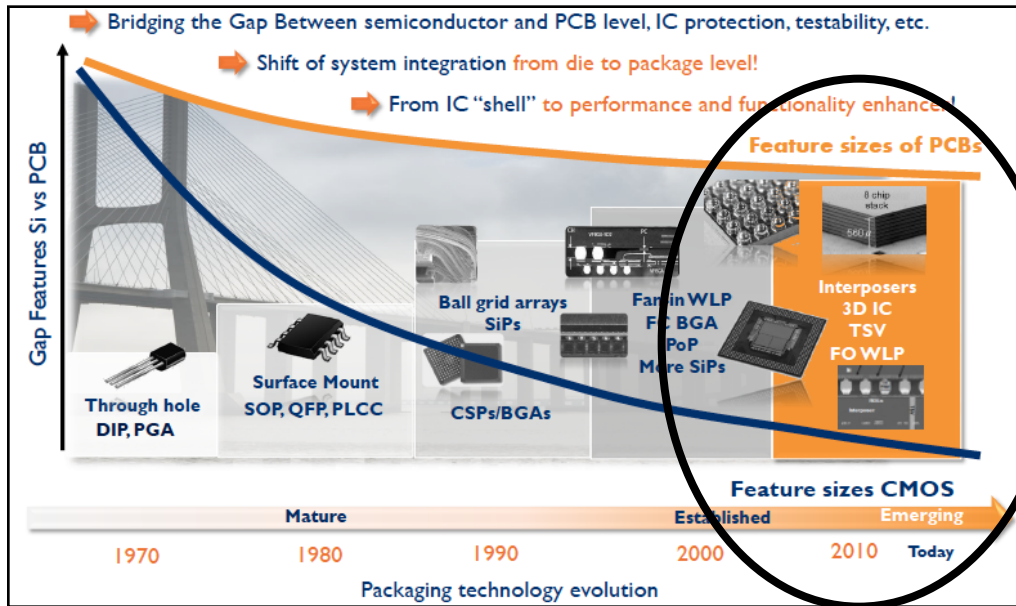
**System OEM
Driven**

System Module



Advanced Packaging Provides a Solution

- Package level homogenous and heterogeneous integration enables the next level of performance



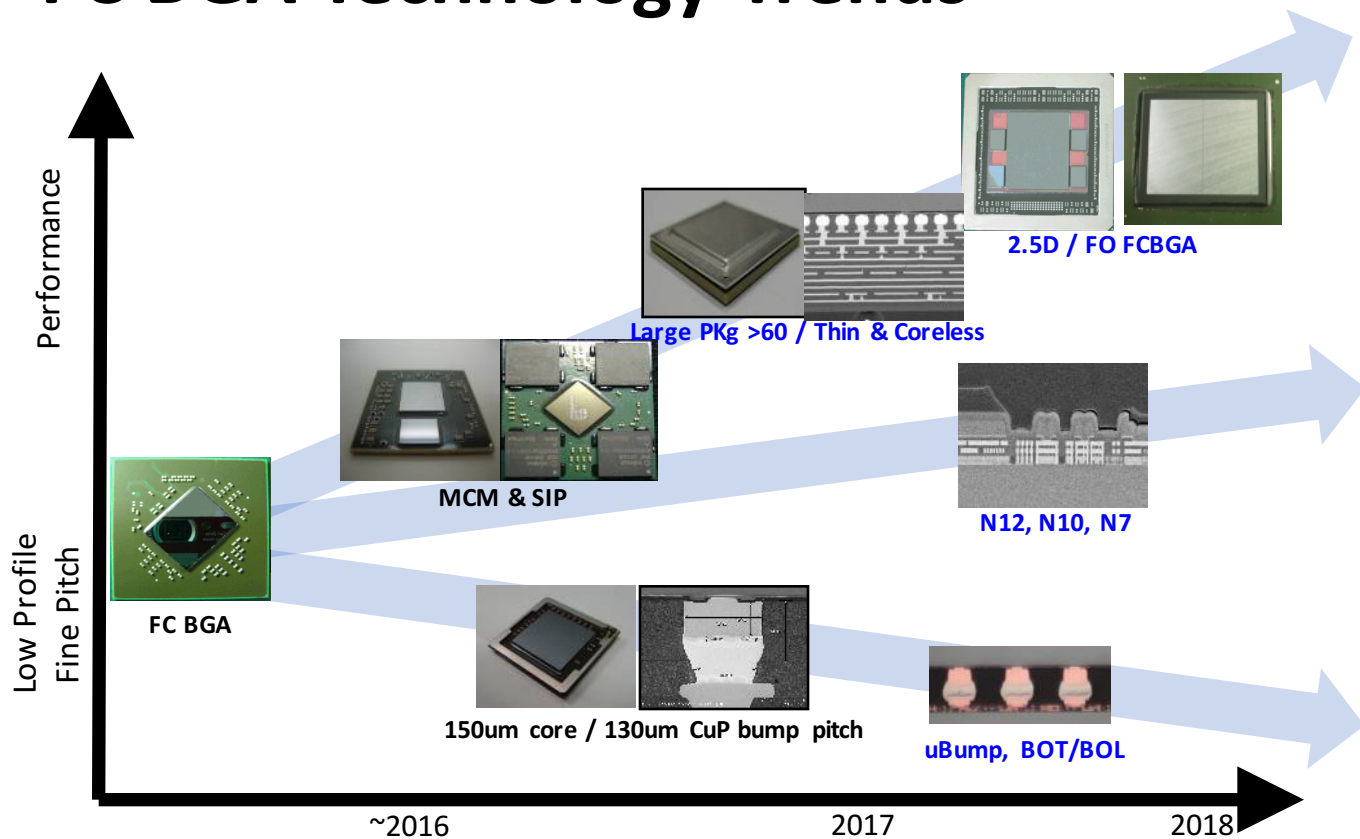
Source: Yole, 3D / 2.5D
Business Update - 2017

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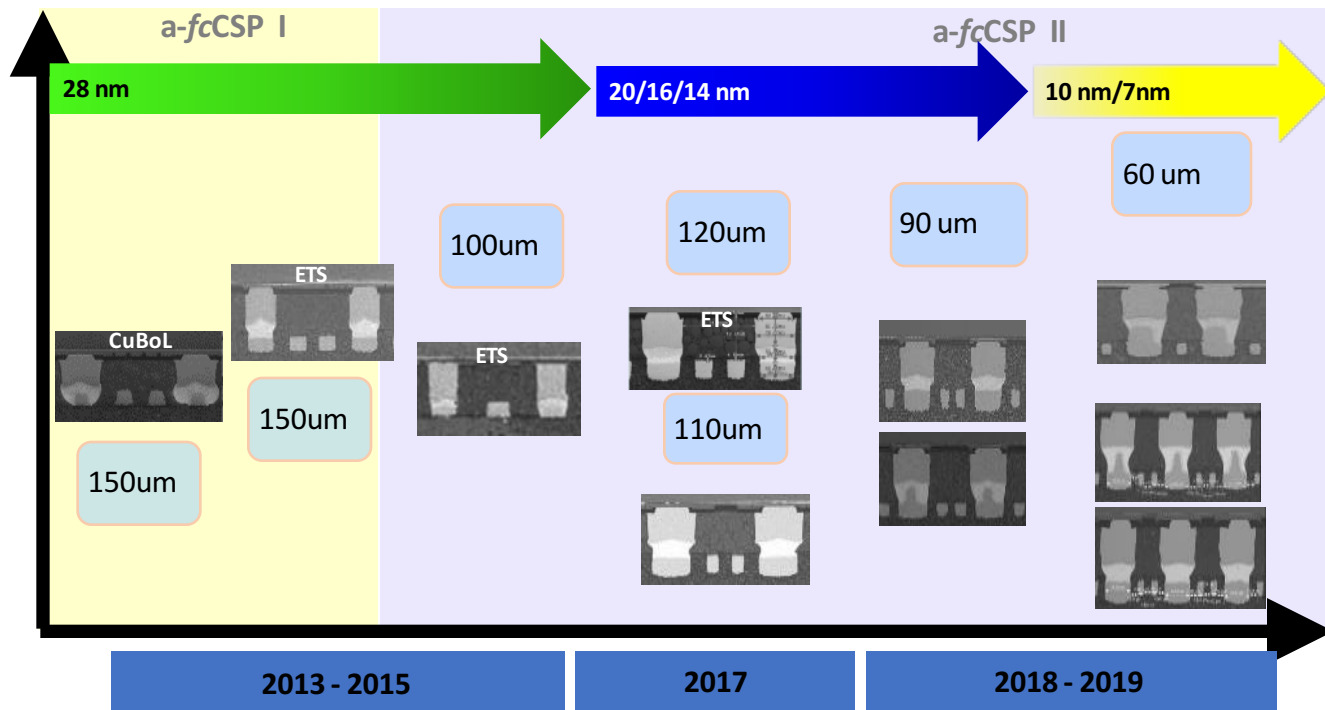


FC BGA Technology Trends



Mobile - Fine Pitch Capability

- Advantage of ETS on fine pitch



Drivers for 2.5/3D Integration



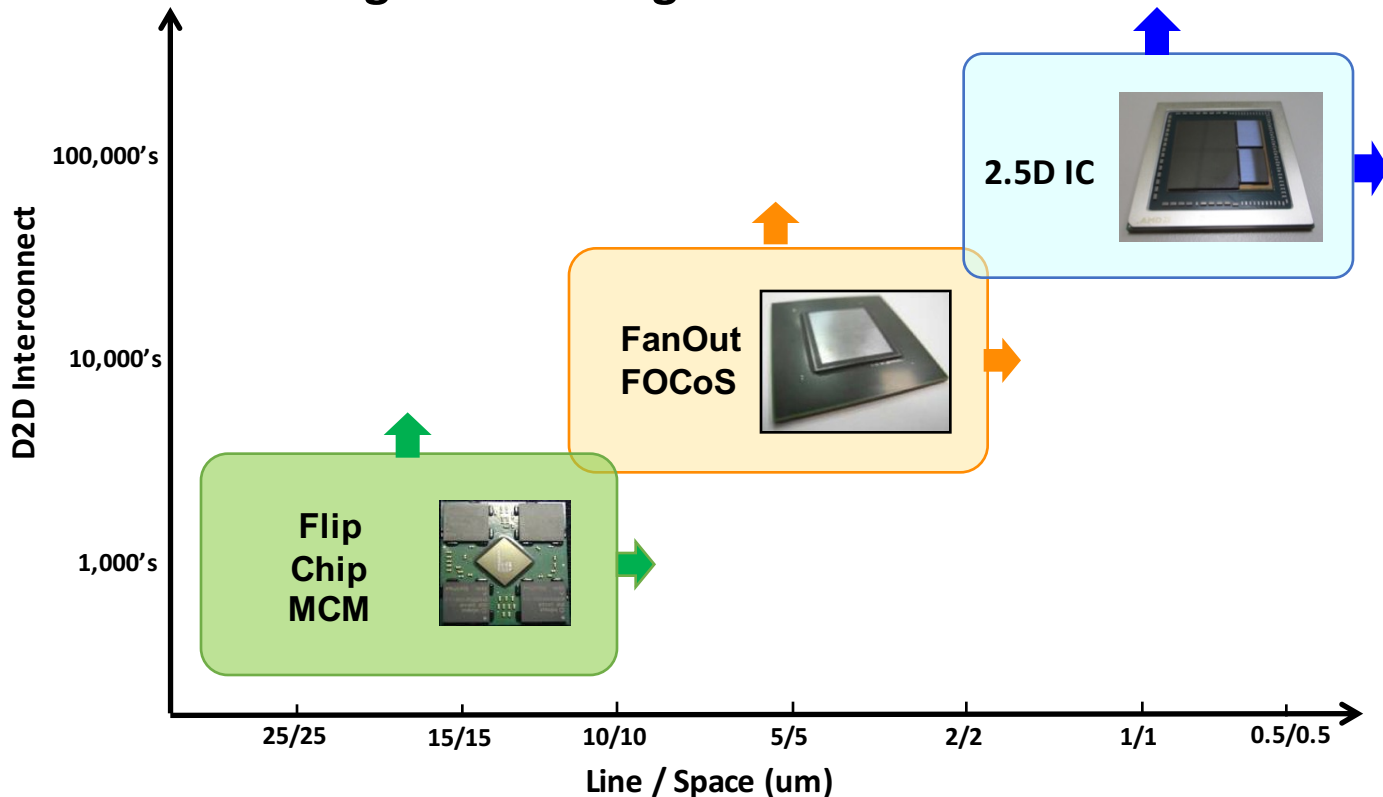
	ICT & networking	High performance computing for data analytics	Consumer computing (gaming + AR/VR)	Aerospace and defense	Automotive computing	Medical computing
Memory cube	x	x	x	x		
Silicon interposer	x	x	x	x	x	x
3D System-on-Chip *	x		x			
Silicon photonics	x	x		x		x

Source: Yole 2.5D/3D Business Update 2017

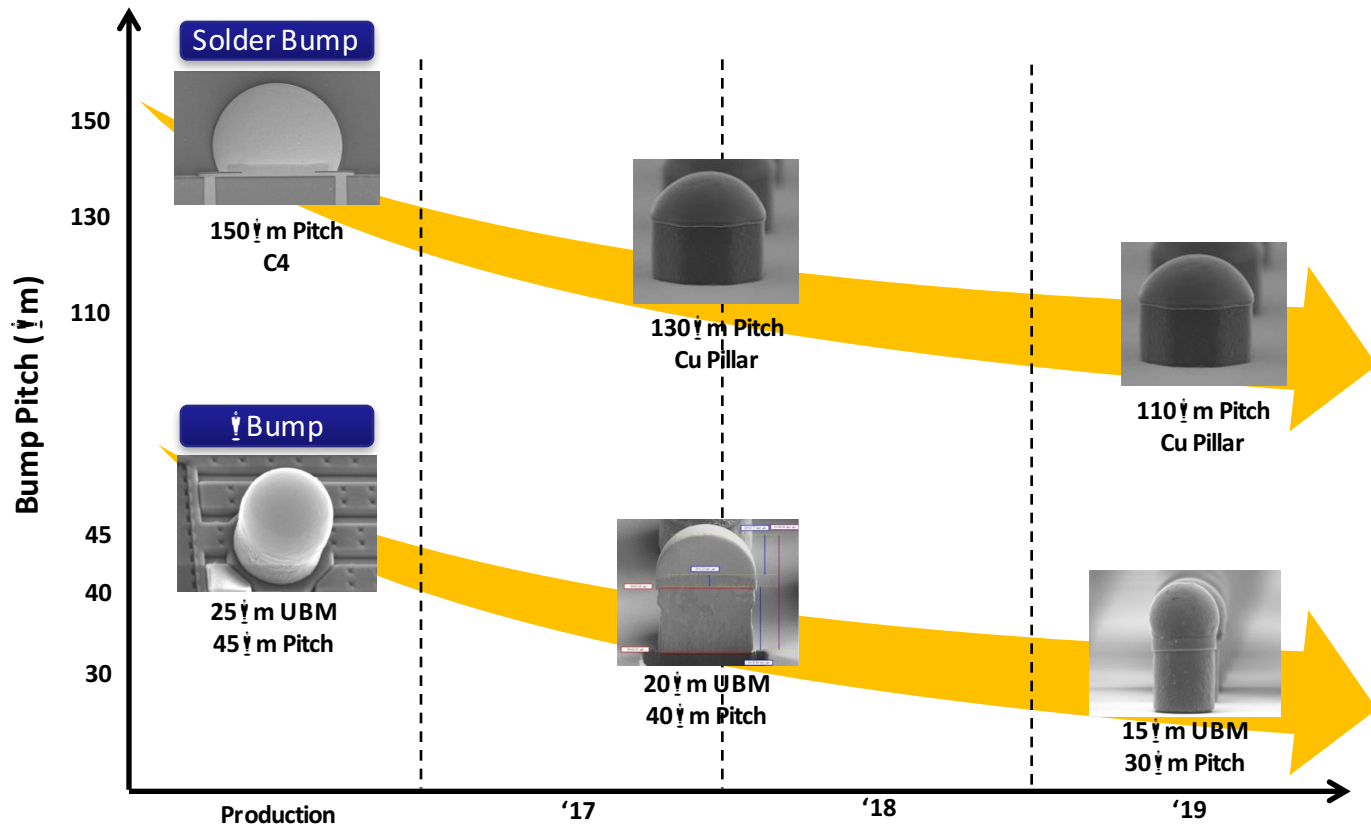
- Higher performance
- Increased bandwidth
- Lower latency
- Reduced power consumption
- Integration of mixed nodes & functionality
- Yield / cost optimization

Addressing High End Integration

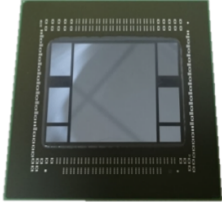
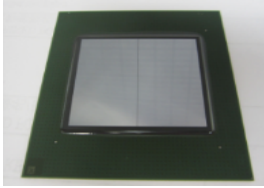
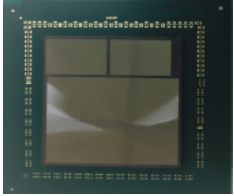
2.5D IC Package Positioning



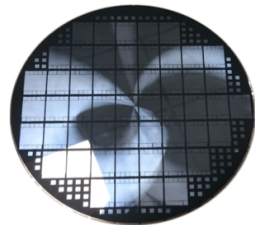
Solder Bump & Microbump Roadmap



Molded 2.5D IC

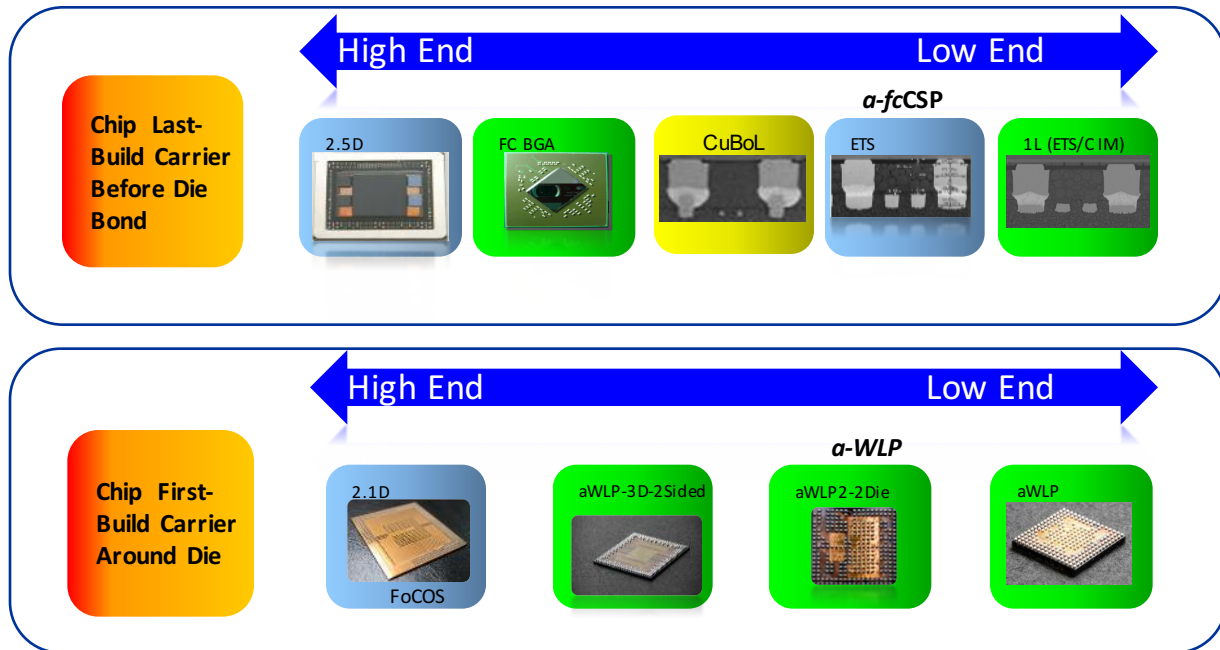
Test Vehicle			
Package Description	Package: 55x55 ASIC + HBM x4 ASIC: 26x22 mm Interposer: 36x28 mm	Package: 55x55 mm ASIC x2 ASIC: 29x18 mm (x2) Interposer: 38x31 mm	Package: 47.5x47.5 ASIC + HBM x2 ASIC: 26x19 Interposer: 30x28 mm

Production Ready



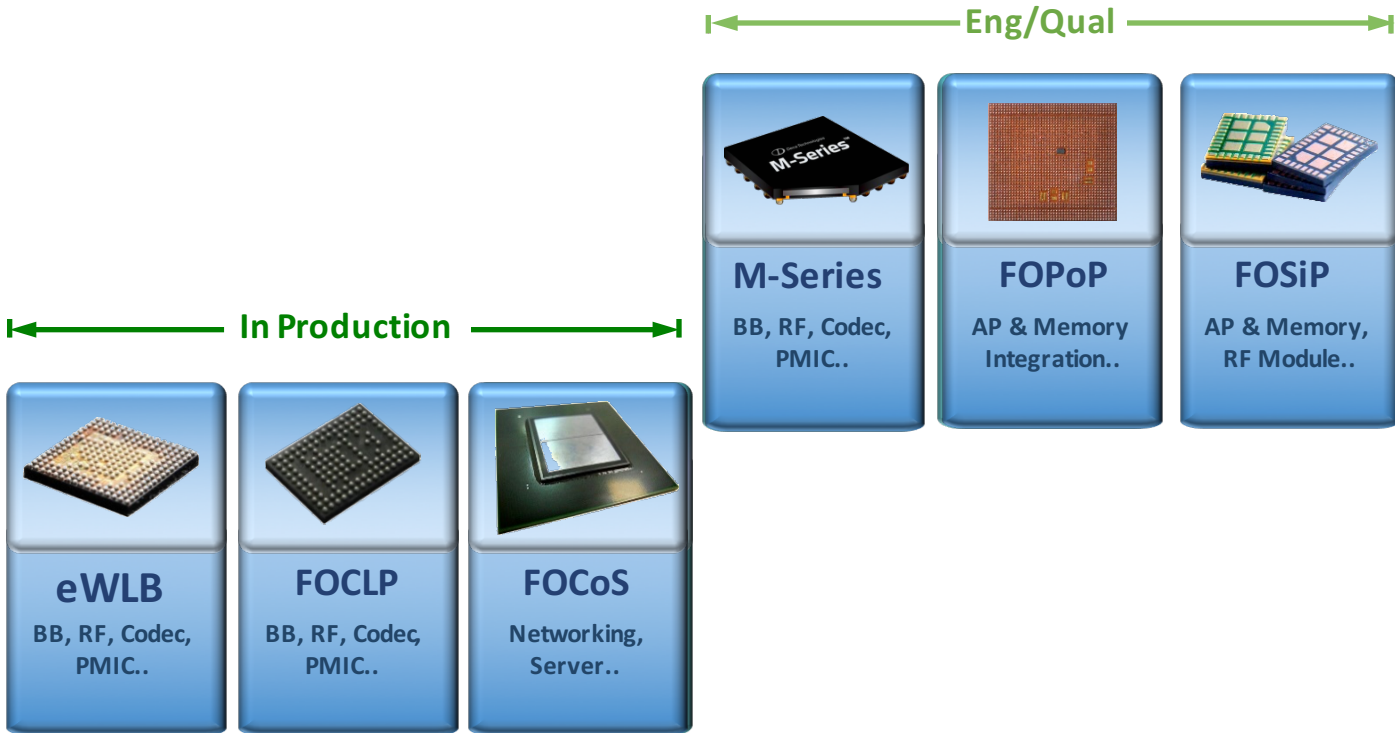
Competitive Solutions

Flip Chip and Fan Out Platforms

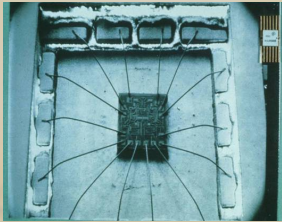


Superior price / performance will win!

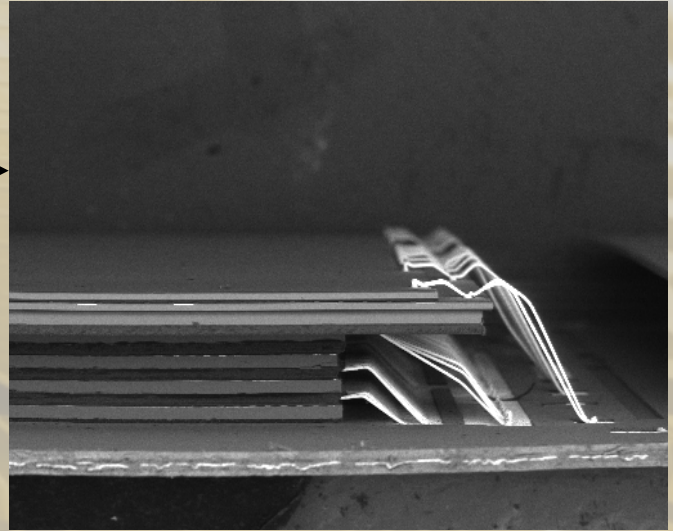
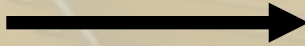
ASE Fan-out Package Platform



Wirebond Technology Is Still Advancing



1967



2017

- Mature
- Reliable
- Easy to use
- HUGE capacity
- Low Cost

Sensor & SiP Solutions Focus



Industrial



Wearable



Medical



Home

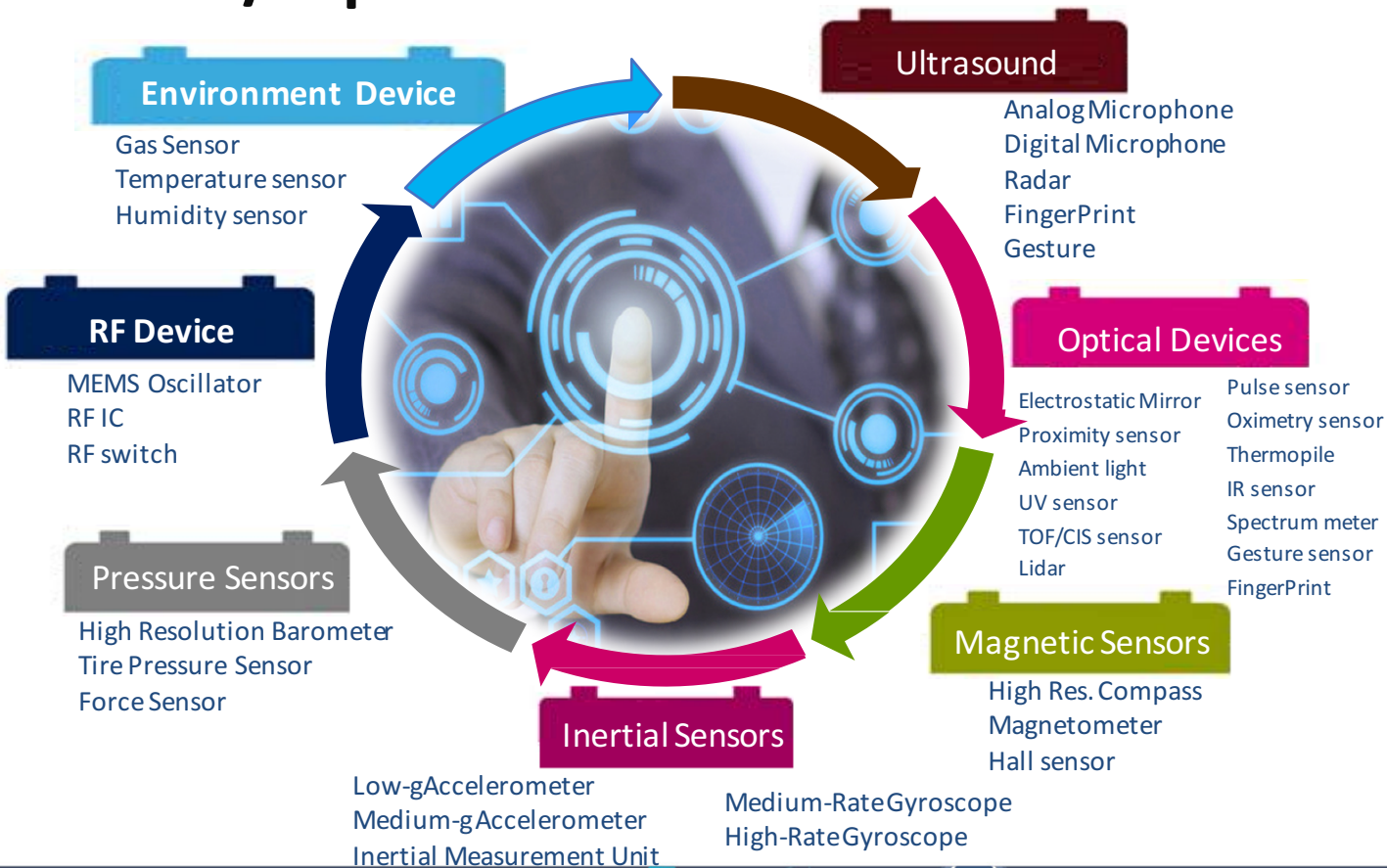


Consumer

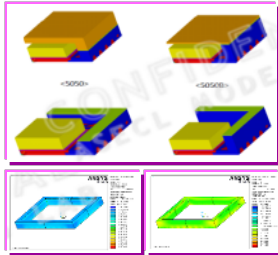


Automotive

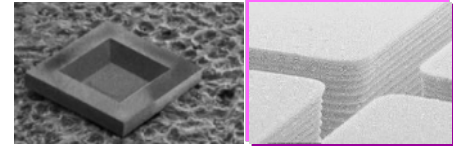
MEMS / Optical Sensors



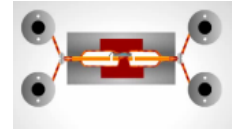
MEMS/Sensor Tool Box



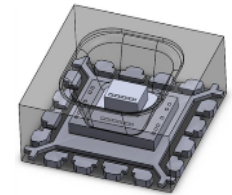
- Stealth laser dicing
- Plasma dicing



**Innovative
Dicing Technology**



**Various
Molding Technology**



- Stress Lab
- Thermal Lab
- Electrical Lab
- Optical lab
- Material Lab

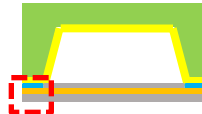
**Simulation
Package Design
New materials**

MEMS

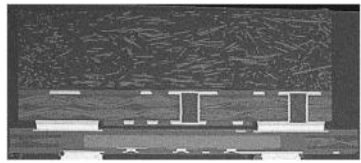
**Embedded
Substrate
Solution**

EMI Technology

- FAM : OCQFN, PMQFN
- Compression molding
- Transfer molding

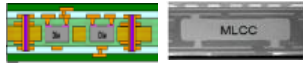


- Plastic lid metallization
- Metal lid w/ different coating technology

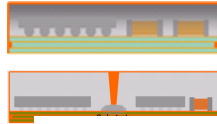


- Active/passive component embedded
- Integrated IPD and MEMS solution
- SESUB solution

SiP Core Technologies



Embedded Technology



Shielding



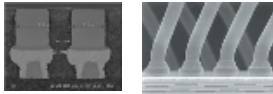
Antenna



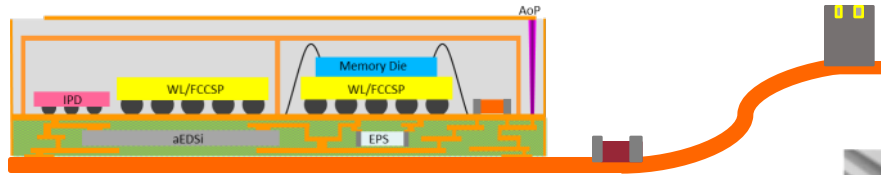
Mechanical Assy



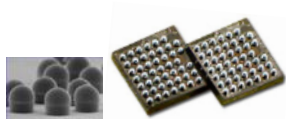
SMT



Interconnection



Die / Pkg Stacking



Wafer Bumping / WLP



POG / IPD



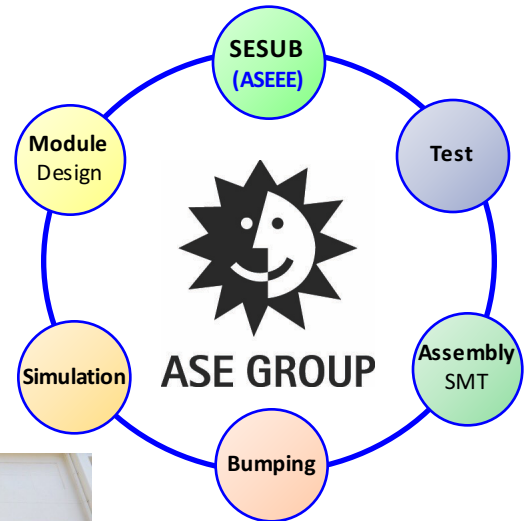
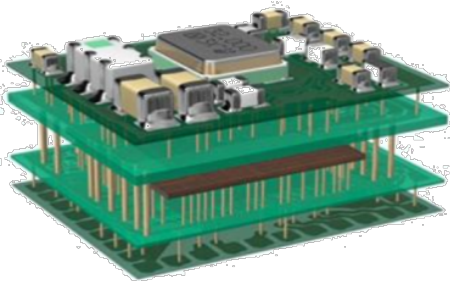
Molding

What We'll Cover

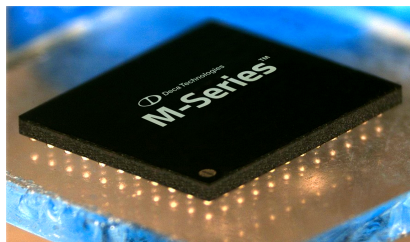
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Collaboration – TDK and ASEEE JV



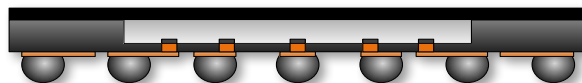
M-Series – Low Density Chip First Die Up



ASE GROUP



Deca Technologies



Chip First Die Up

SiP Intelligent Design

The Next Generation of SiP Design Tool

- ✦ ASE Group collaborates with Cadence on SiP-*id* solution that addresses the design/verification challenges of complex layout of advanced packages, including ultra-complex SiP, Fan-Out and 2.5D packages

Standard Design Flow

Aggregation wafer-, package-and system-level design requirement

Open Design Tool

Yield simulation based on design-to-volume database

Faster Design Time

vs. existing tools with manual operation

SiP-*id* (Intelligent Design) Platform

Advanced IC Package Design + Verification Tool from Cadence



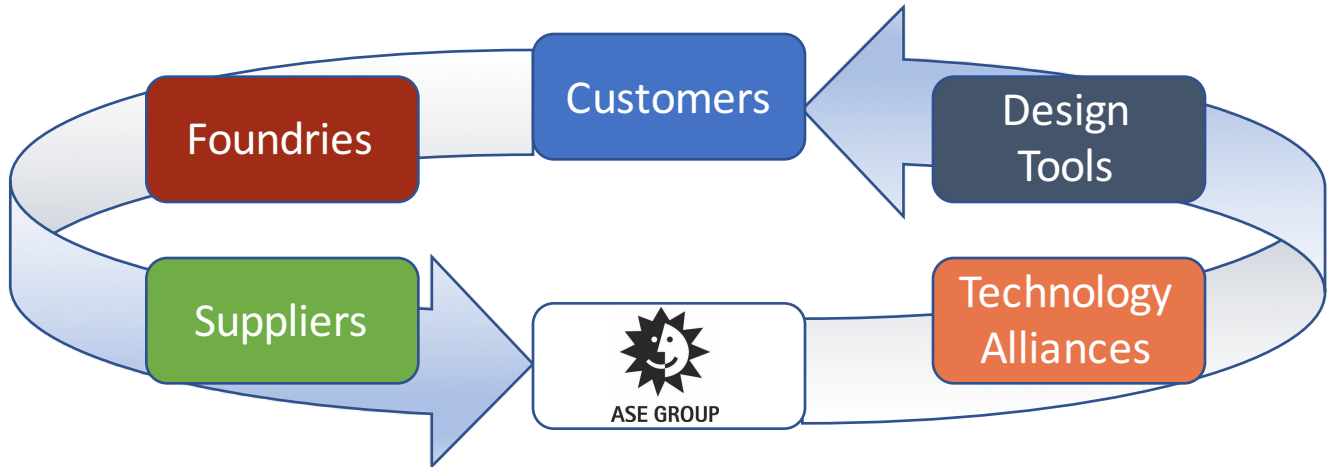
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Key Messages

- Semi growth in 2017, growing but moderating in 2018
- End applications drive very different packaging technologies
- Advancing and leveraging existing packaging platforms
- We must collaborate for success



Thank you



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